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Bridging Domestic Supply and Performance Gaps for the High-Reliability Electronics Industry

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Abstract

Over the past several decades, the consumer electronics industry readily adopted advancements in technology nodes, along with packaging and integration approaches, while also balancing cost of production with increased performance and miniaturization of the product/package. In contrast, the High Reliability (Hi-Rel) microelectronics industry (aerospace, defense, space, medical, energy, and industrial), by necessity, took a conservative and methodical path to qualification and adoption of these new technologies to ensure the robustness and lifetime longevity of the technologies for mission, function, or life critical applications. As a result, the Hi-Rel microelectronics industry usually lags behind the rest of the electronics industry in adopting and ruggedizing new technologies/approaches by 10-15 years, depending on the technology or application. While this approach has worked historically, it is not optimal. By the time a technology is approved for use in a Hi-Rel system, it may already be obsolete or scheduled for end-of-life (EOL) in the high-volume electronics world. More important, several industry factors now threaten to widen the technical performance gap between consumer electronics and Hi-Rel electronics, especially domestically. In this paper, we will discuss industry trends, both technical and economical, and the resulting accessibility and capability gaps. In addition, we will discuss how Micross is addressing these technology and Diminished Manufacturing Sources and Material Shortages (DMSMS)/EOL supply chain challenges to support the performance, form factor, and sustainment needs of the Hi-Rel electronics industry.

Introduction

Over the past two years, there has been growing support in the United States to invest in on-shoring (or re-shoring) of electronics manufacturing, especially as the COVID-19 pandemic highlighted the global supply chain dependency and economic impact of country shutdowns, workforce reduction (people retiring early or leaving the workforce), and decreased industrial output. Chip shortages are well documented and will continue in 2022 with global widespread impact [1, 2]. Even today, most U.S. car dealerships are less than half full with new cars and lead times on new vehicles are on the order of months. Material shortages persist within the microelectronics industry, causing longer lead times for things like ferro-fluidics, stainless steel, processing chemicals, etc. In many cases, spikes in COVID-19 cases in the country of origin are directly affecting supply of raw materials. However, even before COVID-19, technical, economic, and environmental factors had already created accessibility and capability gaps for the Hi-Rel electronics industry, especially domestically. All of which are motivating U.S. government on-shoring initiatives like Creating Helpful Incentives to Produce Semiconductors (CHIPS) for America Act and US Innovation and Competition Act (USICA).

General Microelectronics Industry Factors

For the better part of five decades, the semiconductor industry followed Moore's Law in its pursuit of more performance through higher density integration of transistors in integrated circuits. As technical challenges associated with realizing the next technology node have become more costly and lengthy to overcome, only the largest IC foundries have continued on in pursuit of the next nodes (7 nm and below). In parallel, the industry began looking at advanced packaging and heterogeneous integration techniques as a way to maintain the trajectory of Moore's Law, in terms of functional performance. More recently, there has been a lot

of focus on disintegration of functional blocks from a system on a chip and re-integration through advanced packaging and assembly of "chiplets" into a multichip module (MCM). The high-volume consumer electronics market readily adopted technology advancements, which included increased processing power from higher transistor densities, mated with advanced packaging approaches that squeezed out additional performance gains. Major fabless device companies and 1st tier, vertically integrated foundries and OSATs have driven much of the adoption. In parallel, the U.S. government was also investing in the development and implementation of heterogeneous integration strategies. The holistic approach to design that spans front-end to back-end, enables an overall reduction in size, weight, and power (SWaP). Eventually, the cost sensitivity of the consumer electronics markets drove the manufacturing of these technologies to migrate to lower cost, offshore (outside U.S.) facilities. In fact, today, there are only a handful of U.S. foundries and non-captive advanced packaging suppliers, and even fewer that are U.S. owned and operated [3]. Further, the most advanced IC technology nodes are only available in 300mm wafer formats, with many legacy nodes having migrated from 200mm wafer formats to 300mm wafer formats for improved productivity and efficiency. Last, as through-Si via (TSV) fabrication was developed by foundries in the most recent nodes, blind TSVs (vias-middle) are only available from foundries in their most advanced nodes (i.e. 300mm wafer formats). Advanced Packaging suppliers had no choice but to follow suit and become 300mm wafer-compatible. Where the ROI was not financially feasible (smaller volumes) to add 300mm capability, as compared to consumer electronics, Hi-Rel Advanced Packaging suppliers were left with coring 300mm wafers down to 200mm wafers to be compatible with their processing lines so the required wafer finishing (TSV reveal and addition of off-chip interconnects) could be completed.

For the Advanced Packaging community, the environmentally driven Restriction for Hazardous Substances (RoHS) directives of 2002 and 2011 forced a change in solder metallurgy used for wafer level packaging [4, 5]. Introduced by the European Union, the directive required heavy metals, like lead (Pb), as well as several hazardous flame-retardants, be substituted with safer alternatives. In 2011, the scope extended to all electrical and electronic equipment with full product compliance by July 2019. The removal of Pb from electronic products resulted in the development of Pb-free interconnect metallurgies like SnAg and, ultimately, the elimination of Pb-based solder offerings from most advanced packaging suppliers. While the RoHS directives were necessary for the consumer electronics industry to be environmentally responsible, the fallout from these directives was limited or no availability of Pb-based solders for the Hi-Rel community.

High Reliability Electronics Factors

The Hi-Rel microelectronics part of the industry works in an environment where the device, technology, or system cannot fail and must endure for the lifetime of its mission or purpose. The specific requirements can vary by application, but they all need some degree of ruggedness and longer-term reliability, which drives more rigorous testing, qualification, and cost before approval and deployment of a technology. In many cases, Hi-Rel qualification can take years, while the consumer electronics world may have moved on from that technology and already be on to the next innovation (e.g. cellphone turnover rate of 2-3 years). Because of the time and cost invested in qualifying a technology, the Hi-Rel industry would like 10-15 years of runway before supplanting the technology with a newer technology. For example, Pb-based leads and device interconnects were previously qualified for Hi-Rel applications and any change in material must meet or exceed the qualification standard. As a result, the Hi-Rel community continues to use Pb-based solder and leads, while mainstream electronics have gone Pb-free to comply with RoHS directives. The inherent differences between Hi-Rel and mainstream electronics "product"

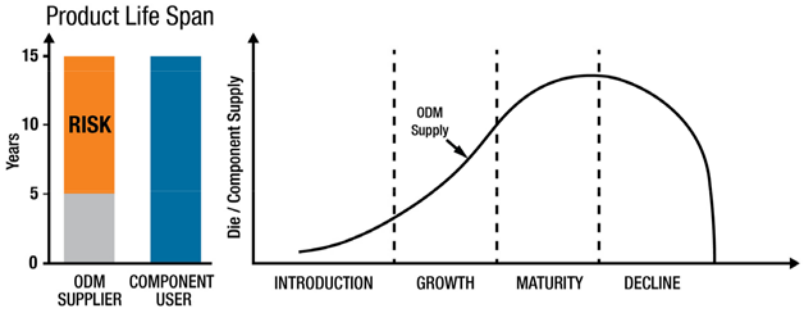

Figure 1: Illustration of differences in ODM product life span and the component user's needed lifespan (left) with typical ODM product life cycle (right).

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lifecycles also means the Hi-Rel applications have to worry about product or platform sustainment as components become obsolete or suppliers declare production end-of-life (EOL) for a technology (Figure 1). Finally, the volumes of wafers, components, or packages needed to support most Hi-Rel applications are typically orders of magnitude below consumer electronics volumes.

Accessibility and Domestic Capability Gaps

The lower volumes associated with Hi-Rel electronics applications are the biggest contributor to the Hi-Rel industry's inability to access state-of-the art devices, packaging, and Si interposers from the largest foundries and OSATs, which focus on serving high volume manufacturing customers and markets. The same access issue exists for start-up companies and emerging technologies, unless they have tangible volumes forecast. Domestically, multi-project wafer (MPW) runs provide some cost effective access to IC manufacturing, but there are a limited number of runs per year and currently little or no access to the most advanced nodes (7 nm and below). Due to RoHS regulations, there has also been a decreasing number of vertically integrated foundries, OSATs, and post CMOS processing providers continuing to offer Pb-based interconnects. Domestically, there are even less providers that offer both wafer-level packaging and 3D heterogeneous integration (3DHI). Moreover, if an application is ITAR restricted, the options are much more limited.

The general industry factors discussed above have contributed to a number of domestic capability gaps. Offshore migration of device and OSAT manufacturing means most of the 300mm processing facilities are offshore, resulting in the absence of a credible onshore, non-captive, 300mm post CMOS processing provider for WLP and wafer finishing. Offshore migration of OSAT manufacturing also means that all of the Fan-Out WLP manufacturing and majority of substrate (organic and ceramic) manufacturing is offshore. If implementing a 3DIC solution in a legacy node, a vias-last TSV insertion, there are only a handful of domestic providers with prototyping capability. Increasing the Manufacturing Readiness Level (MRL) to support manufacturing volumes requires investment in domestic infrastructure. Similarly, the domestic supply chain for Si and glass interposers needs maturation to improve onshore accessibility and availability.

Providing a Domestic Solution

Micross Components has been supporting the Hi-Rel industry for over 40 years, striving to address the accessibility, domestic capability, and sustainment challenges through its value streams (see Figure 2). Micross' die distribution business has an extensive bare die line card and IDM access that allows us to help identify, procure, and supply devices (bare die or packaged) to the industry. Relationships with our IDMs provide Micross device access that one-time buyers or low volume customers cannot obtain. A key part of the value stream is the EOL die sustainment program (EDSP), which supports Hi-Rel customers in avoiding costly redesign/re-qualification and mitigating counterfeit risk. By understanding customer program/platform lifetime needs and leveraging its supplier relationships, Micross helps manage the supply of and storage of parts (die or wafer format) needed to support programs to their desired Hi-Rel end date (Figure 3).

Through a combination of pre-existing and acquired business units (Micross AIT, Micross Hi-Rel, Micross STS), Micross has built itself into a Hi-Rel electronics OSAT. The Advanced Interconnect Technology (AIT) business unit at Micross provides high value added, post-CMOS wafer processing services for the fabrication of advanced interconnects on active (CMOS, photonic, III-V, etc. devices) and passive (Si and glass

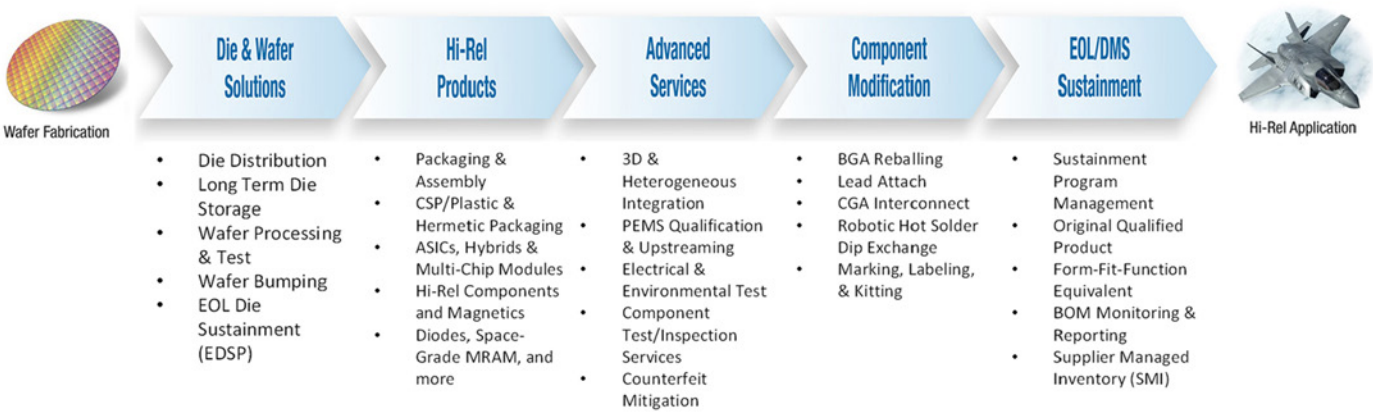

Figure 2: Micross Components value streams of products and services for the Hi-Rel industry.

interposer) wafers that enable finished devices/die to go into advanced package architectures (flip-chip packages, 2.5D packages, and 3DHI stacks). The advanced interconnect design, process, and fabrication knowledge include design and fabrication for both wafer-level packaging (WLP) and 3D heterogeneous integration (HI) technologies on a 200mm compatible backend line with flexibility for smaller wafer formats (e.g. 100mm and 150mm), which is important for III-V substrates utilized in high power RF and mm-wave devices. For WLP, off-chip interconnects ranging from electroplated C4 solder bumps (PbSn eutectic, high Pb, and Pb-free), copper pillar, ball drop for WLCSP, and electroplated micro-bumps (sub-20 um pitch Au, In, Cu-based) are available, along with copper redistribution layers (RDL) and Ni/Au receiving and wire bond pads (see Figure 4a for example of eutectic bump plus Cu RDL). For 3DHI, Micross AIT offers both TSV and through-glass via (TGV) processing to support post-CMOS TSV insertion (example in Figure 4b) and wafer finishing, as well as advanced substrate fabrication (Si interposers or glass interposers). While Micross does not have frontend-of-line (FEOL) process capability for the high density routing required for many interposer applications, our relationships with other members of the domestic ecosystem (frontend foundries and design partners) can provide a reliable supply chain for these types of substrates. Similarly, Micross Hi-Rel has good standing relationships with ceramic and organic substrate vendors for other advanced packaging solutions. Micross is actively working with U.S. stakeholders to address the 300mm WLP and wafer-finishing gaps, with plans to add these capabilities to the AIT business unit. Establishing domestic access to FOWLP and hybrid bonding capabilities is on the Micross technology roadmap as well.

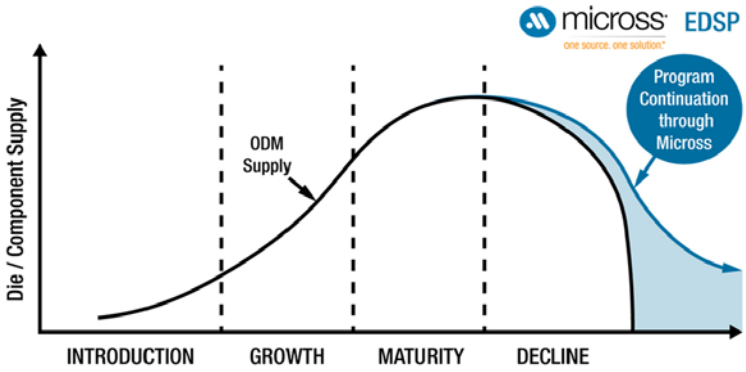

Figure 3: Micross sustaining Hi-Rel platforms past original device manufacturers EOL.

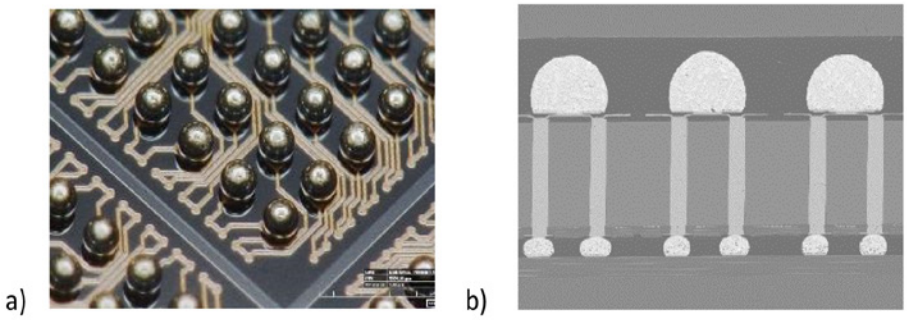

Figure 4:
a) C4 bump + RDL for fan-in example; b) TSV insertion in active CMOS for 3DHI solution example.

Combined, the Hi-Rel Components and Micross STS business units provide packaging, assembly, and final test services (Figure 5). Packaging capabilities include hermetic packaging (ceramic and metal can), plastic packaging (CSP, BGA, QFN), customer packaging, flip-chip packaging, multichip modules (MCM), and system in package (SIP). End-to-end service and support from package design to full package characterization, to turnkey assembly and test are available. Automated and state-of-the-art die attach, wire bond, encapsulation and CSP capabilities allow us to provide solutions for a broad range of technologies and applications, from single die packages to electro-optic MCMs. When it comes to electrical testing, an array of experience, technical expertise, and equipment provide a full range of performance validation services for precision high-performance ICs used in analog, digital, mixed and RF signal processing applications. For the most demanding applications, Micross has a suite of environmental and test chambers to accelerate deterioration and shorten test cycles by varying temperature and pressure. Capabilities include high and low temperature operating limits (HTOL/LTOL), highly accelerated stress test (HAST), high temperature storage life (HTSL), temperature humidity bias (THB), ESD characterization and many others. Our facilities allow us to provide qualification at the component or board level to verify and validate packages or components for Hi-Rel applications.

Within Micross' Component Modification Services business, there is extensive expertise and capability to modify existing packages to meet Hi-Rel standards. Pb-free solder balls can safely be replaced with higher reliability tin-lead balls through a BGA re-balling process (Figure 6, left image). Issues like Sn whiskers can be eliminated through replacement of Sn with tin-lead finish through a robotic hot solder dip (RHSD) and exchange process (Figure 6, right image). Complementary capabilities exist in lead attach and trim and form.

Micross is also expanding its design capability for advanced packages and 3DHI solutions by building out an internal design team. A key to that capability is developing strong relationships with the EDA vendors to help vet and improve the EDA tools for design and modeling of advanced packages. As a non-captive service provider, Micross plans to establish relationships with several EDA vendors to ensure the tools support both mainstream OSAT and Hi-Rel OSAT capabilities and needs.

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Figure 5:
Examples of packaging and advanced test capabilities available from Micross Hi-Rel and Micross STS business units.

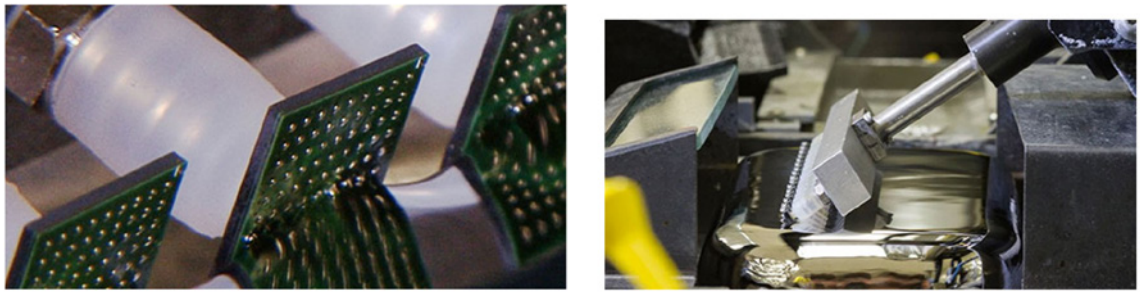

Figure 6: BGA re-balling (left image) and Robotic Hot Solder Dip (RHSD) modification of a package (right image).

Summary

Technical, environmental, and economic electronics industry factors have widened the domestic capability and accessibility gap for the Hi-Rel electronics industry. Resolving the problem is complex, because it spans the manufacturing supply chain from frontend foundry to advanced packaging and assembly, making it impossible to address with a single entity solution. Know-how and technical capability still exist onshore, but a sustainable domestic solution will require an ecosystem of government, key stakeholders (e.g. the Hi-Rel industry), and existing domestic microelectronics supply chain working together. As part of the existing supply chain, Micross Components is actively working with stakeholders and other members of the domestic ecosystem to expand domestic capabilities, internal and external, to be a key part of the domestic solution. U.S. government initiatives like USICA and CHIPS for America Act will accelerate the time to get there, and enable a more robust, self-sustaining, domestic solution.

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